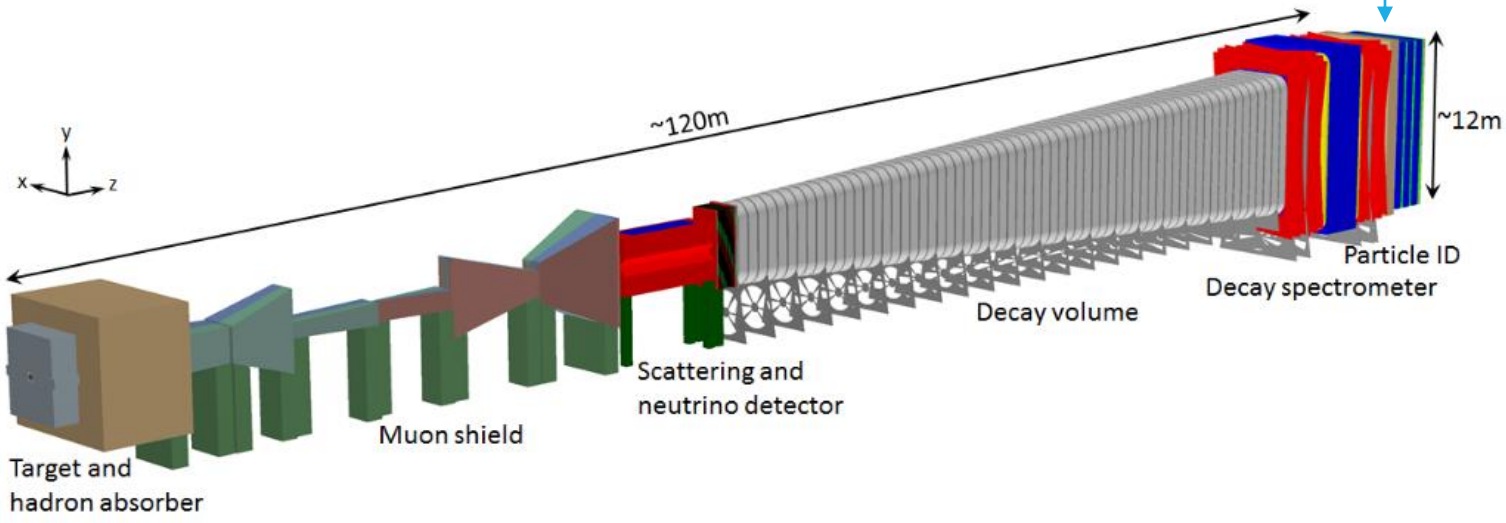
SHiP

INFN Istituto Nazionale di Fisica Nucleare Sezione di Bologna

The SHiP Muon Detector

Detector Overview

The muon detector sits at the very end of the SHiP experiment



It identifies muons and provides a timing measurement for background suppression

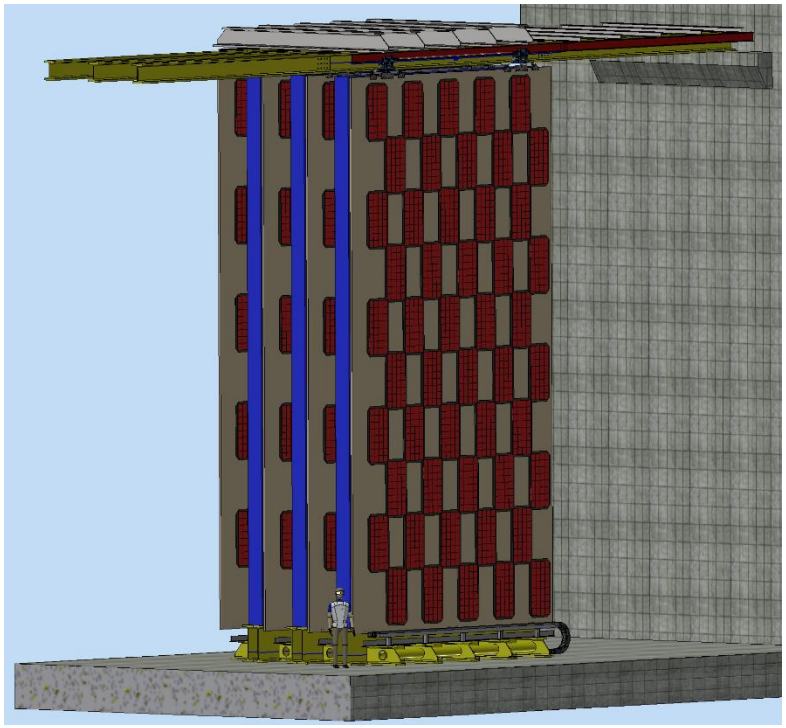
Detector Overview

Requirements:

- very high (> 99.5%) identification efficiency for muons (p > 3 GeV/c)
- pion misidentification < 0.1%
- high time resolution (~ 200 ps)
- spatial resolution of ~ 10 cm

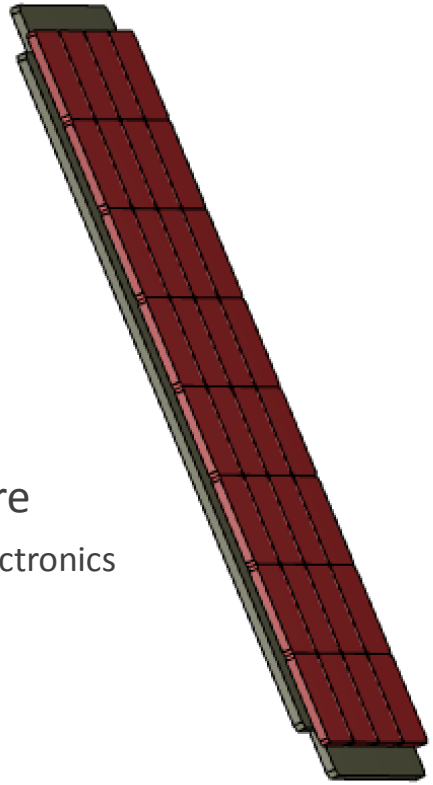
Layout:

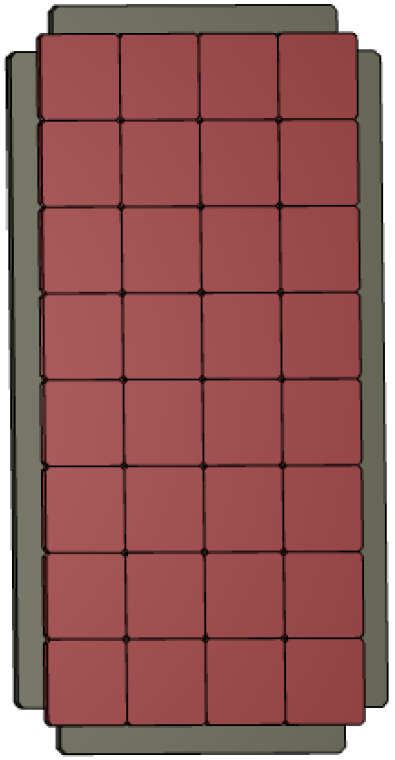
- Four active layers, 6 by 12 m
  - On a sliding wall for easy access
  - Staggered checkerboard on both sides
- Three passive absorber layers
  - Investigating iron and concrete



Detector Module

- 32 Scintillator tiles
  - 60x120 cm total
- Light-tight enclosure
  - Includes front end electronics
- 400 Modules
  - ~13000 tiles

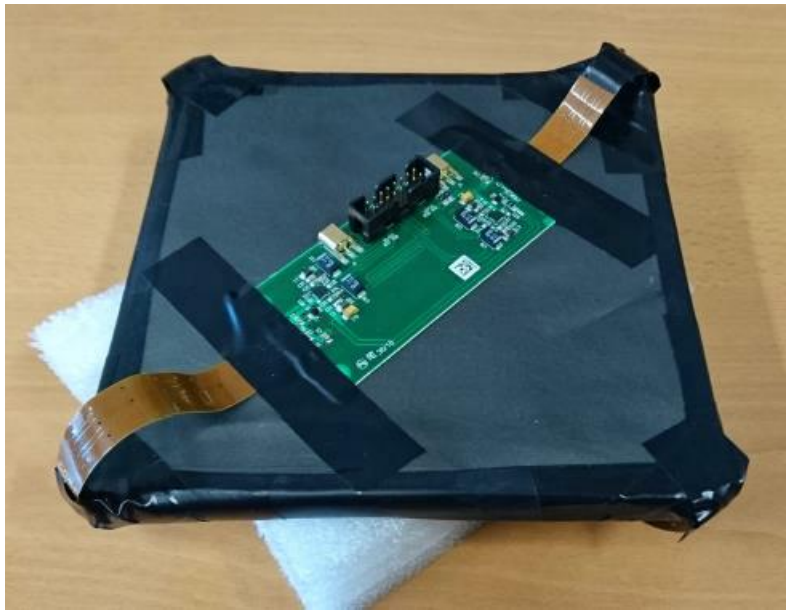




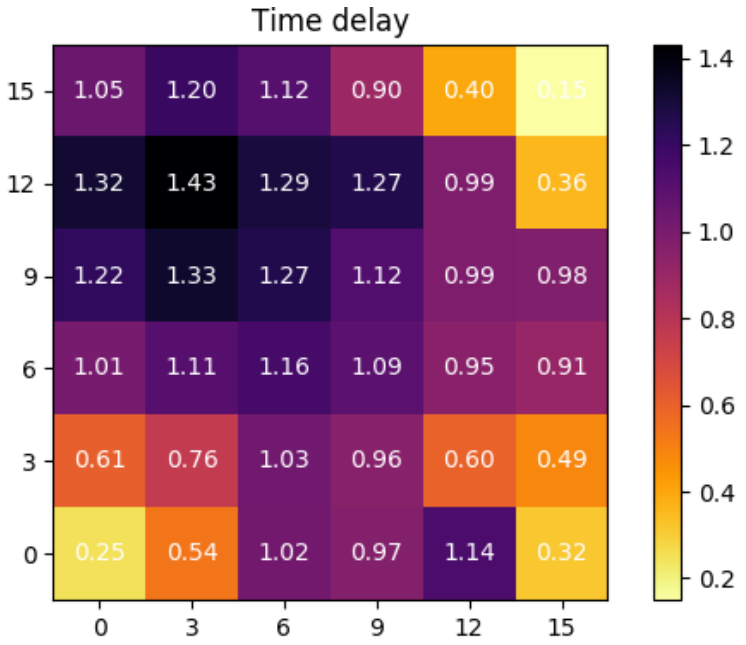
Scintillator tile

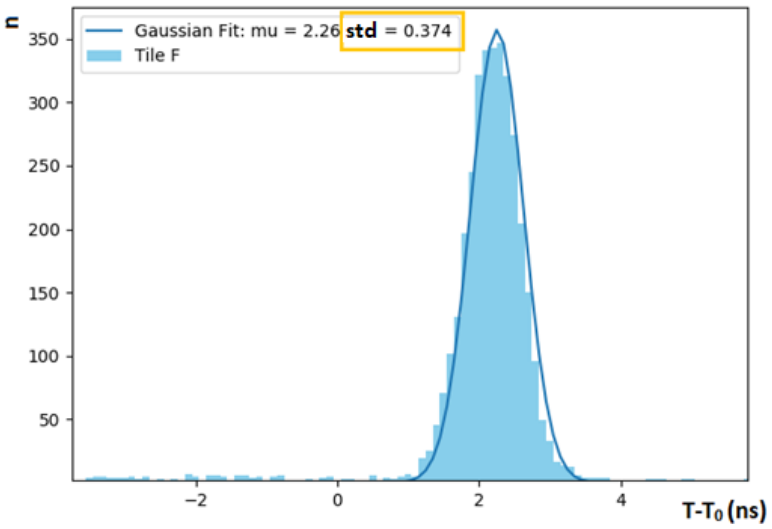
- EJ-200 plastic scintillator
- 15 x 15 x 1 cm
- White diffusive paint coat
- Hamamatsu SiPMs 4 x 4 mm
- SiPMs mounted in each corner
- Analog electronics on tile

Latest tile prototype



Latest results



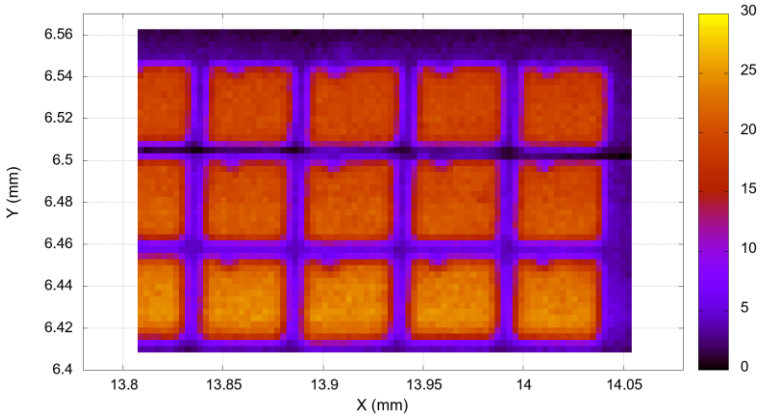


As low as 350 ps on a tile
Now aiming for < 300

Refining the design - hardware

Finalizing the tile design

- Choice of final SiPM
- Choice of wrapping/coating
- SiPMs mounting position
  - e.g. slots look more promising than corners

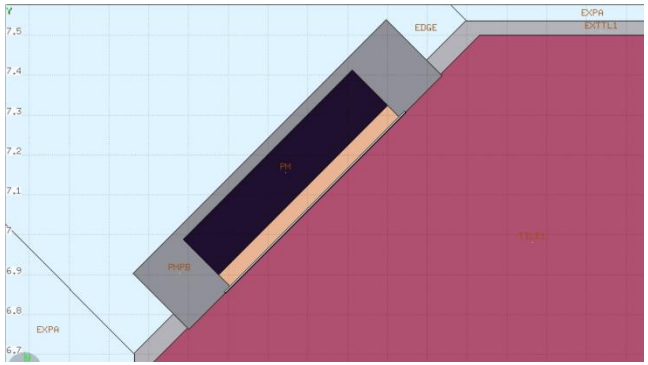


Trying to develop better SiPMs:

- FBK, lower crosstalk, larger SiPM
- Preselected for AIDA++ funds

Refining the design - simulation

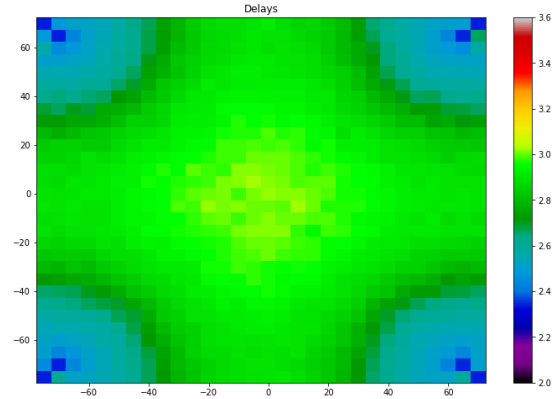
FLUKA tile model by Tiziano



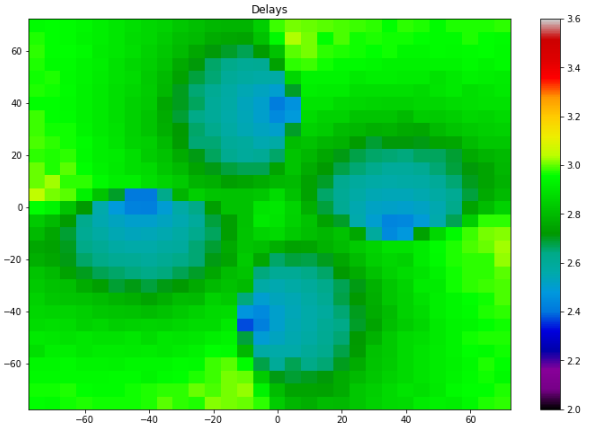
Closely reproduces measurement

Allows to study many different configurations quickly

Corners



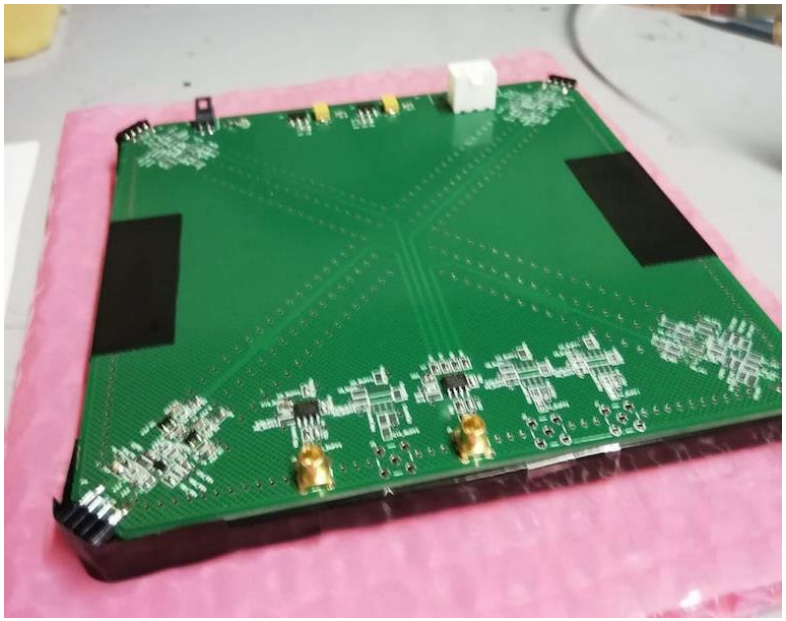
Cross



Analog electronics

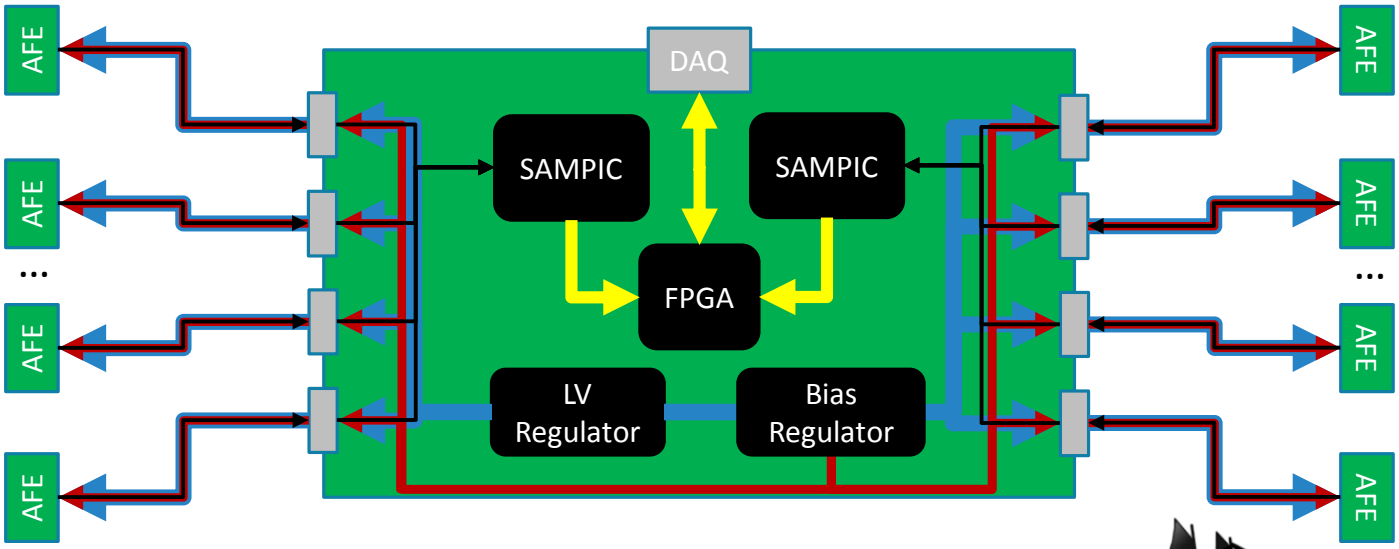
- High bandwidth preamplifier
  - One per SiPM
  - Single BJT, common base
  - > 1 GHz
- Linear adder
  - Sum of four analog inputs
  - Reduces the number of channels
  - Preserves pulse shape information

Latest electronics prototype (LNF)

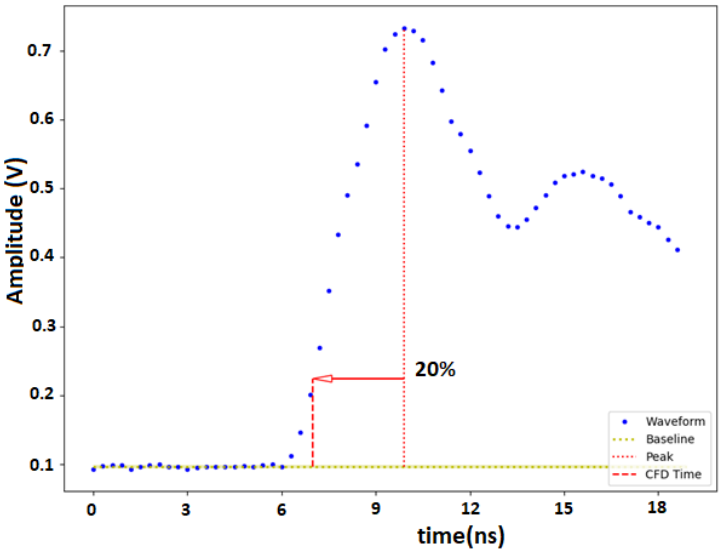


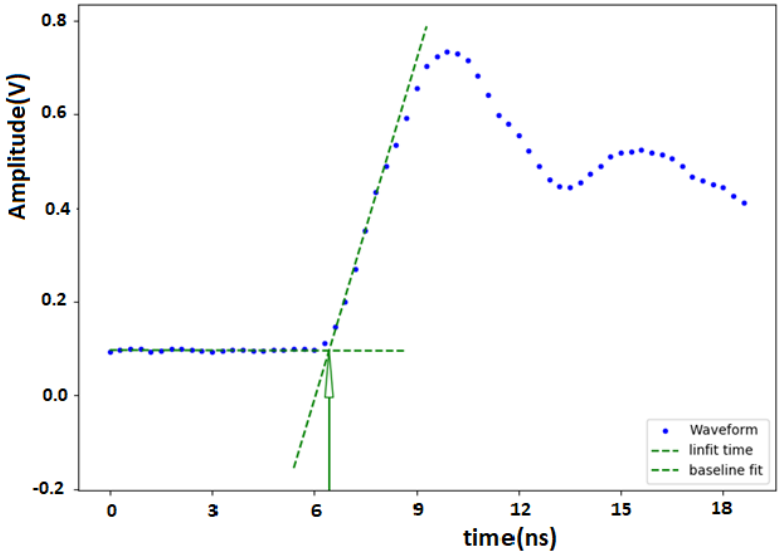
Digital electronics

- SAMPIC: 64 cell analog memory digitizer, made by LAL-Orsay
  - Samples rising edge at 3.2 GSps -> waveform information
  - 16 channels, low cost and low power
- One 32 channel board per module, with all services



Data analysis





Testing conventional (CFD) and improved algorithms for timestamping